CLAIMS

What is claimed is:

1.   A freeway routing system for a field programmable gate array (FPGA), the

FPGA comprising:

5   a plurality of FPGA tiles, each FPGA tile comprising:

             a plurality of functional groups (FGs) arranged in rows and

columns;

             a plurality of interface groups (IGs) surrounding said plurality of

FGs such that one IG is positioned at each end of each row and column, each of

10   the IGs having a first, second and third set of input ports and a first, second and

third set of output ports;

a freeway set of routing conductors configured to transfer signals to the first,

second and third input ports of IGs in one FPGA, and configured to transfer

signals from said first, second and third output ports of the IGs of all other FPGA

15   tiles;

             said freeway set of routing conductors comprising:

                    a plurality of vertical conductors that form intersections with

a plurality of horizontal conductors; and

                    programmable interconnect elements located at said

20   intersections in a diagonal orientation on said FPGA tile.

2.   The FPGA of Claim 1, wherein said FPGA further comprises:

        at least one other FPGA tile configured in the same manner as said

first FPGA;

        wherein the freeway set of routing conductors of each FPGA tile

are connected to any adjacent FPGA tile's freeway set of routing conductors.

3.   The FPGA of Claim 2, wherein said FPGA further comprises:

        programmable interconnect elements located at said connections

between adjacent FPGA tiles.

4.   The FPGA of Claim 1, wherein said diagonally oriented programmable

interconnects are arranged from the upper left corner of said first FPGA tile to the

lower right corner of said first FPGA tile.

5.   The FPGA of Claim 1, wherein said diagonally oriented programmable

interconnects are arranged from the upper right corner of said first FPGA tile to

the lower left corner of said first FPGA tile.

6.   The FPGA of Claim 1, wherein said freeway set of routing conductors are

further configured to also transfer signals from output ports of at least one IO.

7.   The FPGA of Claim 1, wherein said freeway set of routing conductors are

further configured to also transfer signals from output ports of at least one RAM.

8.   A method of routing the internal components in a FPGA tile comprising:

        inputting a function netlist defining a user circuit;

optimizing said user circuit;

placing user cells defining said user circuit into said FPGA internal

components;

using a first set of routing conductors to route said user circuit to

5   interconnect said internal components to implement said user circuit; and

engaging a freeway set of routing conductors to meet said user

circuit routing requirements;

generating a programming bitstream defining said user circuit; and

programming said FPGA functional unit with said bitstream to

10   implement said user circuit.

9.   A method of routing the internal components in a FPGA tile comprising:

inputting a function netlist defining a user circuit;

optimizing said user circuit;

placing user cells defining said user circuit into said FPGA internal

15   components;

using a first set of routing conductors and a freeway set of routing

conductors to route said user circuit to interconnect said internal components to

implement said user circuit;

generating a programming bitstream defining said user circuit; and

programming said FPGA functional unit with said bitstream to

implement said user circuit.

10.   A method of providing a freeway interconnect structure in a FPGA

comprising:

5   providing a plurality of FPGA tiles;

providing a plurality of functional groups (FGs) arranged in rows

and columns on each said FPGA tile;

providing a plurality of interface groups (IGs) surrounding said

plurality of FGs such that one IG is positioned at each end of each row and

10   column, each of the IGs having a first, second and third set of input ports and a

first, second and third set of output ports;

providing a freeway set of routing conductors configured to

transfer signals to said first, second and third input ports of IGs of one FPGA tile,

and configured to transfer signals from said first, second and third output ports

15   of IGs of all other FPGA tiles;

said act of providing a freeway set of routing conductors

comprising:

providing a plurality of vertical conductors that form

intersections with a plurality of horizontal conductors; and

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providing programmable interconnect elements located at

said intersections in a diagonal orientation on said FPGA tile.

11.   The method of Claim 10 further comprising:

providing at least one other FPGA tile configured in the same

5   manner as said first FPGA; and

connecting said freeway set of routing conductors of each FPGA

tile to any adjacent FPGA tile's freeway set of routing conductors.

121.   The method of Claim 11, further comprising:

providing programmable interconnect elements located at said

10   connections between adjacent FPGA tiles.

13.   The method of Claim 10, further comprising configuring said freeway set

of routing conductors to also transfer signals from output ports of at least one

IO.

14.   The method of Claim 10, further comprising configuring said freeway set

15   of routing conductors to also transfer signals from output ports of at least one

RAM.

15.   An apparatus for routing the internal components in a FPGA tile

comprising:

means for inputting a function netlist defining a user circuit;

20   means for optimizing said user circuit;

means for placing user cells defining said user circuit into said

FPGA internal components;

means for using a first set of routing conductors to route said user

circuit to interconnect said internal components to implement said user circuit;

5   means for determining whether the routing requirements of said

user circuit have been met using said first set of routing conductors;

means for engaging a freeway set of routing conductors to meet

said user circuit routing requirements;

means for generating a programming bitstream defining said user

10   circuit; and

means for programming said FPGA functional unit with said

bitstream to implement said user circuit.

16.   An apparatus for routing the internal components in a FPGA tile

comprising:

15   means for inputting a function netlist defining a user circuit;

means for optimizing said user circuit;

means for placing user cells defining said user circuit into said

FPGA internal components;

means for using a first set of routing conductors and a freeway set of routing conductors to route said user circuit to interconnect said internal components to implement said user circuit;

means for generating a programming bitstream defining said user circuit; and

means for programming said FPGA functional unit with said bitstream to implement said user circuit.